
AFRL-AFOSR-VA-TR-2016-0054

# Nanopillar Photonic Crystal Lasers for Tb/s Transceivers on Silicon

**Diana Huffaker**
**UNIVERSITY OF CALIFORNIA LOS ANGELES**

**07/09/2015**
**Final Report**



Air Force Research Laboratory
AF Office Of Scientific Research (AFOSR)/ RTA1
Arlington, Virginia 22203
Air Force Materiel Command

# REPORT DOCUMENTATION PAGE

*Form Approved*
**OMB No. 0704-0188**



| 1. REPORT DATE *(DD-MM-YYYY)* | 2. REPORT DATE | 3. DATES COVERED *(From - To)* |
|---|---|---|
| 30-00-2015 | Report Type - Annual | March 2014 - March 2015 |

**4. TITLE AND SUBTITLE**
Nanopillar Photonic Crystal Lasers for Tb/s Transceivers on Silicon

**5a. CONTRACT NUMBER**
FA9550-12-1-0052

**5b. GRANT NUMBER**

**5c. PROGRAM ELEMENT NUMBER**

**6. AUTHOR(S)**
Huffaker, Diana L

**5d. PROJECT NUMBER**

**5e. TASK NUMBER**

**5f. WORK UNIT NUMBER**

**7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)**
University of California at Los Angeles
420 Westwood Plaza, Engineering IV
Los Angeles, CA, 90095

**8. PERFORMING ORGANIZATION REPORT NUMBER**

**9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)**
Air Force Office of Scientific Research

**10. SPONSOR/MONITOR'S ACRONYM(S)**
AFOSR

**11. SPONSORING/MONITORING AGENCY REPORT NUMBER**

**12. DISTRIBUTION AVAILABILITY STATEMENT**
Public, No Restrictions

DISTRIBUTION A

**13. SUPPLEMENTARY NOTES**

**14. ABSTRACT**

The objective of this project is the development of materials and devices to be used in next-generation Tb/s optical transceivers on Silicon substrates. This project has focused on a unique approach to growth of III-V emitters via selective-area epitaxy (SAE). The first year of the project focused on development of electrical injection of NP emitters. This work was successful in demonstrating electroluminescence in NP-LEDs at 1.3μm. Due to the combination of axial current injection and radial surface passivation, the NP-LEDs are the first such devices based on nanowires or NPs which exhibit optical and electrical properties that are similar to their planar counterparts. The NP-LEDs were further developed by the introduction of axial diffusion barriers comprised of GaAsP inserts. Detailed characterization of growth of the GaAsP inserts and electronic band-offset measurements were used to effectively implement the GaAsP inserts as diffusion barriers. The implementation of these barriers in NP-LEDs demonstrated a five-fold increase in output intensity, making this a promising approach to high-efficiency pillar-based emitters in the near-infrared wavelength range.

**15. SUBJECT TERMS**

| 16. SECURITY CLASSIFICATION OF: | | | 17. LIMITATION OF ABSTRACT | 18. NUMBER OF PAGES | 19a. NAME OF RESPONSIBLE PERSON |
|---|---|---|---|---|---|
| a. REPORT | b. ABSTRACT | c. THIS PAGE | | 9 | 19b. TELEPONE NUMBER (*Include area code)* |
| x | | | | | |

INSTRUCTIONS FOR COMPLETING SF 298

**1. REPORT DATE.** Full publication date, including day, month, if available. Must cite at lest the year and be Year 2000 compliant, e.g., 30-06-1998; xx-08-1998; xx-xx-1998.

**2. REPORT TYPE**. State the type of report, such as final, technical, interim, memorandum, master's thesis, progress, quarterly, research, special, group study, etc.

**3. DATES COVERED**. Indicate the time during which the work was performed and the report was written, e.g., Jun 1997 - Jun 1998; 1-10 Jun 1996; May - Nov 1998; Nov 1998.

**4. TITLE.** Enter title and subtitle with volume number and part number, if applicable. On classified documents, enter the title classification in parentheses.

**5a. CONTRACT NUMBER**. Enter all contract numbers as they appear in the report, e.g. F33615-86-C-5169.

**5b. GRANT NUMBER.** Enter all grant numbers as they appear in the report, e.g. 1F665702D1257.

**5c. PROGRAM ELEMENT NUMBER.** Enter all program element numbers as they appear in the report, e.g. AFOSR-82-1234.

**5d. PROJECT NUMBER.** Enter al project numbers as they appear in the report, e.g. 1F665702D1257; ILIR.

**5e. TASK NUMBER.** Enter all task numbers as they appear in the report, e.g. 05; RF0330201; T4112.

**5f. WORK UNIT NUMBER.** Enter all work unit numbers as they appear in the report, e.g. 001; AFAPL30480105.

**6. AUTHOR(S).** Enter name(s) of person(s) responsible for writing the report, performing the research, or credited with the content of the report. The form of entry is the last name, first name, middle initial, and additional qualifiers separated by commas, e.g. Smith, Richard, Jr.

**7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES).** Self-explanatory.

**8. PERFORMING ORGANIZATION REPORT NUMBER.** Enter all unique alphanumeric report numbers assigned by the performing organization, e.g. BRL-1234; AFWL-TR-85-4017-Vol-21-PT-2.

**9. SPONSORING/MONITORS AGENCY NAME(S) AND ADDRESS(ES).** Enter the name and address of the organization(s) financially responsible for and monitoring the work.

**10. SPONSOR/MONITOR'S ACRONYM(S).** Enter, if available, e.g. BRL, ARDEC, NADC.

**11. SPONSOR/MONITOR'S REPORT NUMBER(S).** Enter report number as assigned by the sponsoring/ monitoring agency, if available, e.g. BRL-TR-829; -215.

**12. DISTRIBUTION/AVAILABILITY STATEMENT.** Use agency-mandated availability statements to indicate the public availability or distribution limitations of the report. If additional limitations/restrictions or special markings are indicated, follow agency authorization procedures, e.g. RD/FRD, PROPIN, ITAR, etc. Include copyright information.

**13. SUPPLEMENTARY NOTES.** Enter information not included elsewhere such as: prepared in cooperation with; translation of; report supersedes; old edition number, etc.

**14. ABSTRACT.** A brief (approximately 200 words) factual summary of the most significant information.

**15. SUBJECT TERMS.** Key words or phrases identifying major concepts in the report.

**16. SECURITY CLASSIFICATION.** Enter security classification in accordance with security classification regulations, e.g. U, C, S, etc. If this form contains classified information, stamp classification level on the top and bottom of this page.

**17. LIMITATION OF ABSTRACT.** This block must be completed to assign a distribution limitation to the abstract. Enter UU (Unclassified Unlimited) or SAR (Same as Report). An entry in this block is necessary if the abstract is to be limited.

# Annual Project Report

**Executive Summary:** The objective of this project is the development of materials and devices to be used in next-generation Tb/s optical transceivers on Silicon substrates. This project has focused on a unique approach to growth of III-V emitters via selective-area epitaxy (SAE). The use of SAE growth at nanoscale dimensions avoid defect formation due to lattice mismatch by allowing strain relief in the lateral direction. By this method, high uniformity arrays of III-V nanopillars (NPs) were successfully grown on Si (111) substrates. Previous work on NPs was successful in developing both axial and radial heterostructures by control of growth conditions, leading to demonstrations of GaAs/InGaAs axial heterostructures for optical gain and GaAs/InGaP radial heterostructures for *in-situ* surface passivation. The use of SAE growth enabled accurate control of NP placement and geometry so that optical cavities could be formed by the NPs themselves. The combination of these techniques lead to the demonstration of room-temperature continuous wave lasing from NP arrays.

Following the development of waveguide-coupled NP optoelectronic devices which was the focus of the second year of the project, the final year focused on the integration of the NP devices on Silicon substrates. The GaAs seeding layer was studied to achieve high vertical yield and high-uniformity GaAs nanopillars on Si(111) substrates by SAE. Seeding layer growth temperature was optimized to obtain over 99% yield of vertical growth. The nanopillars were passivated by *in-situ* AlGaAs shells to reduce the surface recombination. No threading dislocation and anti-phase domains were observed at Si/GaAs interface by transmission electron microscopy. Moreover, the optical properties of NPs were measured by photoluminescence and time-resolved photoluminescence at room temperature to investigate the effects of seeding layer parameters. Under the optimum conditions, it was found that GaAs NPs on Silicon can have carrier recombination lifetimes in excess of 1 ns, which is comparable to NPs grown on GaAs substrates.

## A. Overview of Seeding-layer Development

Many growth techniques have been developed so far for GaAs-based NWs on Si. One of the most common ways to grow large-scale free-standing GaAs-based NWs on Si is to use vapor-liquid-solid (VLS) mode with the assist of gold (Au) catalyst by metal-organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE). Unfortunately, it suffers from a problem that Au droplets may create the mid-gap defect states in NWs to reduce the carrier lifetime. Another technique is called self-assembled/self-catalyzed growth mode, where NWs are directly grown on non-patterned substrates with or without Ga droplets. However, the uniformity control of NW arrays is insufficient to meet the requirements mentioned above. In this case, selective-area (SA) growth shows its benefits that no alien contamination from catalyst is

introduced, and the positions and dimensions of NWs can be adjusted by lithographically patterned nanoholes on dielectric mask. Some studies of SAE growth on Si using Ga droplets, *i.e.* Ga predeposition, have been reported, but the size of droplets needs to be precisely controlled to avoid multi-twinning during the nucleation that gives tilted NW growth. Instead, we investigate SA-MOCVD using a thin GaAs transition layer, called GaAs seeding layer in this paper, for GaAs-based nanopillars (NPs) on Si. A similar growth technique has been reported by Fukui's group for both GaAs NWs and InAs NWs on Si (111). In our work, we focus on the optimization of the growth condition for GaAs seeding layer to obtain high-uniform and high vertical yield GaAs NP arrays. Further, a great potential of such growth technique is that not only the binary GaAs, but also the ternary GaAs-based NW/NP arrays, can be grown on Si by adding a GaAs seeding layer and using similar growth conditions on III-V substrates for NP segment. Thus, the seeding layer can be considered as an epi-ready layer inside the patterned nanoholes.

In this study, the effects of seeding layer growth temperature on uniformity, vertical yield, and optical properties of NP arrays will be discussed in detail. Also, the Zn-doped GaAs NPs instead of intrinsic GaAs NPs will be investigated, because the material characteristics of doped III-V NWs/NPs on Si have rarely been reported. Between them, the minority carrier lifetime serves as a significant factor to determine the electrical properties for III-V nano-devices on Si. The process of growth pattern preparation and the growth sequence will be given as well. The dimension and vertical yield NP arrays were measured by scanning electron microscope (SEM). The interface of Si substrate and GaAs seeding layer was characterized by transmission electron spectroscopy (TEM), and the bulk NP optical properties were measured by photoluminescence (PL) and time-resolved photoluminescence (TRPL) at room temperature.

**B. Experimental Development of GaAs-NPs on Silicon (111) Substrates**

The substrate used for this growth was lightly boron-doped (resistivity 0.8 – 1.2 Ω-cm) 4-inch on-axis silicon (111) wafer. The surface root-mean-square (RMS) roughness measured by Scanning Probe Microscope (SPM) was 0.14 nm, about half of a Si monolayer along (111). The wafer was firstly cleaned by the standard Piranha and RCA2 followed by BOE oxide-strip for 15 s. A 20 nm silicon nitride ($SiN_x$) film was deposited by low-pressure chemical vapour deposition (LPCVD). LPCVD $SiN_X$ gives higher etch selectivity to native oxide on Si by BOE compared with plasma-enhanced chemical vapour deposition (PECVD) and thermal silicon dioxide ($SiO_2$). Next, E-Beam resist ZEP520A was coated and nanoholes were patterned by E-Beam lithography (EBL). The designed diameter and pitch of nanoholes for EBL patterning are 80 nm and 800 nm, respectively, and the size of the array is 50 $\mu m$ × 50 $\mu m$. The $SiN_x$ layer was etched by reactive-ion etching (RIE) to expose the Si surface. Since the final growth result is sensitive to the cleaning process, we carefully designed the steps to remove the resist. The major part of E-Beam

resist was cleaned by Piranha at 120°C, and the rest was removed by $O_2$ downstream plasma. Right before sample was loaded into MOCVD chamber, the native oxide in the nanoholes was stripped by BOE for 45 s.

The growth of NPs was accomplished using a low-pressure (60 Torr) Emcore MOCVD reactor, where hydrogen ($H_2$) was used as carrier gas. The precursors were Trimethylgallium (TMGa), Trimethylaluminium (TMAl), Tertiarybutylarsine (TBA), and diethylzinc (DEZn). The schematic of growth sequence and structure is illustrated in Figure 1(a) and (b), respectively. At the beginning, the growth chamber temperature was directly ramped up to 870°C for 10 min. During this step, the extra thin native oxide that was formed before sample loading was fully removed by thermal deoxidation. After baking, the temperature was ramped down to the seeding layer growth temperature. Then, TBA was flowed at $1.97\times10^{1}$ sccm for 5 min in order to replace the first layer of Si atoms inside the nanoholes and make As-incorporated $Si^{3+}$ (111)B surface [54]. The seeding layer was grown for a short time 5 s with gas flow of TMGa at $7.55\times10^{-1}$ sccm and TBA at $4.39\times10^{0}$ sccm, and the V/III ratio is 58. After this, the temperature was ramped up to 730°C to carry out vertical Zn-doped GaAs NPs for 7 min. The gas flows of TMGa, TBA, and DEZn during NP growth were $1.13\times10^{-1}$ sccm, $2.14\times10^{1}$ sccm, and $4.31\times10^{-2}$ sccm, respectively. The estimated doping was at the level of $10^{18}$ $cm^{-3}$. Finally, a thin AlGaAs passivation shell was grown at 600 °C, followed by a thin GaAs cap to prevent the oxidation of Al. Different

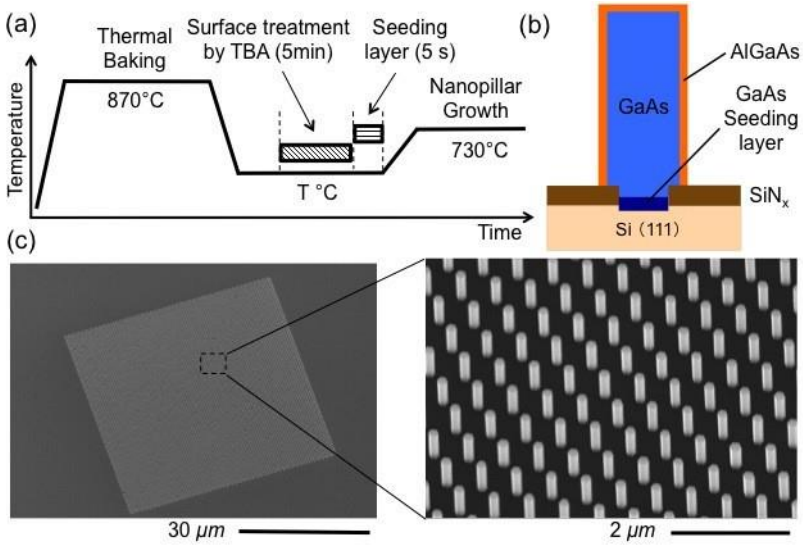


**Figure 1.** (a) Schematic of growth sequence of GaAs NPs on silicon. The AlGaAs passivation shell growth is not shown here. The temperature and growth time are not to scale. (b) The growth structure showing the GaAs seeding layer position. (c) SEM image of the 50 $\mu m$ × 50 $\mu m$ array with over 7000 NPs. The designed diameter and pitch of nanoholes are 80 nm and 800 nm, respectively.

temperature during seeding layer growth was used to investigate the uniformity and vertical yield of NP arrays. As shown in Figure 1(c), the growth patch is a 50 μm × 50 μm array and the number of NPs is over 7000.

The geometry of NPs including height and diameter was evaluated by SEM. FEI T12 TEM was operated in bright field to study the Si/GaAs interface and bulk GaAs NP section. He-Ne laser at 633 nm was used as the pumping source for PL calibration, and the signal was detected by Si visible femtowatt photoreceiver. TRPL measurement was carried out by NKT SuperK EXTREME continuum laser operated at 633 nm with repetition rate 39.01 MHz, MPD Si single photon avalanche diodes (SPADs), and PicoHarp single photon counting.

### C. Optimization of GaAs Seeding Layers for Ultra-High Uniformity

Seeds are always necessary for selective-area GaAs-based NPs on Si to help the nucleation. It is reported that the outmost of Si monolayer along (111) can be reconstructed and replaced by As to form Si(111):As 1×1 by annealing between 300 °C and 450 °C in As ambient. Thus, the starting point of our experiment was to grow seeding layer at 450 °C for a short time 5 s. Low TMGa flow was used to keep slow growth rate. The 30° tilted SEM image of GaAs NPs with 450 °C seeding, as shown in Figure 2(a), gives the yield of vertical growth over 90% despite

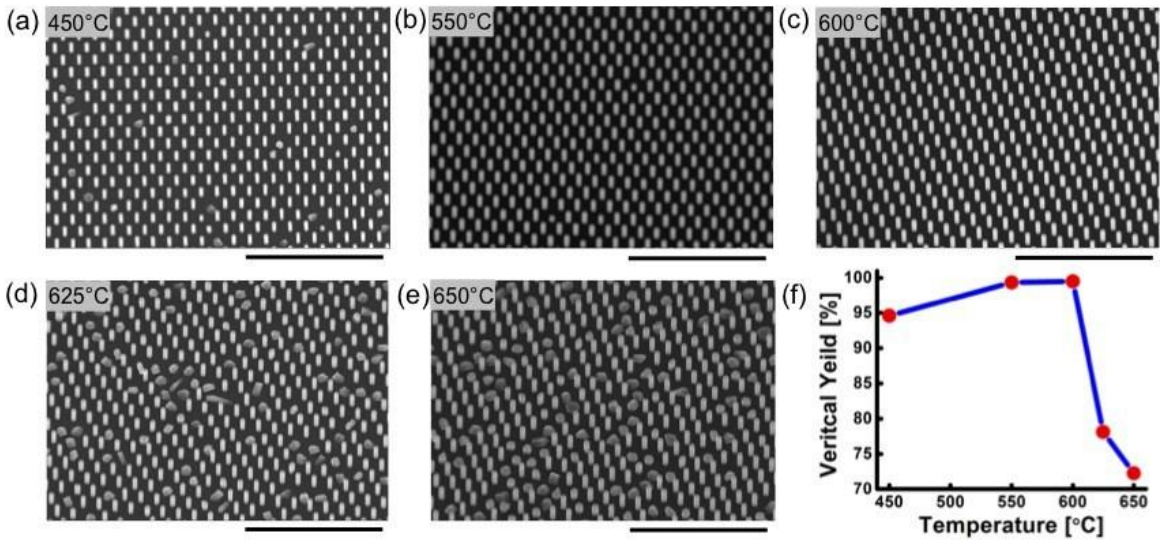


**Figure 2.** 30° tilted SEM images of Zn-doped GaAs NPs on Si. The scale bar for all images is 5 $\mu m$. (a)-(e) Increase of growth temperature for GaAs seeding layer growth: 450 °C, 550 °C, 600 °C, 625 °C, and 650 °C. The growth time of seeding layer is 5 s for all cases. (f) The vertical yield of NPs in the function of seeding layer growth temperature.

some irregular polycrystalline islands structures and tilted NPs randomly located inside the array. The formation of such random imperfect growth may be due to two reasons: (1) the sample is not clean enough and small resist particles stick to the edge of nanoholes; and (2) the multiple nucleations are formed during the seeding layer growth. In our case, the former one is highly possible, because the formation of polycrystalline seeds is sensitive to the growth temperature. Moreover, GaAs matrix grown at low temperature is As-rich and highly nonstoichiometric. Therefore, we increased the growth temperature for seeding layer. As shown in Figure 2 (b)-(e), four different temperatures were applied: 550°C, 600°C, 625°C, and 650°C. It is clearly observed that the uniformity and vertical yield are both improved from 450°C to 600°C, while the density of polycrystalline islands is increased when the temperature is over 600°C. The vertical yield in the function of seeding layer temperature is illustrated in Figure 2(f), where 99.5% yield is achieved by seeds grown at 600°C. The impact of temperature on uniformity and vertical yield is comparable with the reported study on Ga droplet seeds by MBE growth. In our case, the optimized seeding layer temperature is 600 °C. The vertical yield of hexagonal NP growth is over 99%, and the measured average height and diameter of NPs are 760 nm and 150 nm, respectively.

The cross-sectional TEM of GaAs NPs was carried out as shown in Figure 3(a), and the close-up bulk NP section and Si/GaAs interface were also given in Figure 3(b) and (c). It is observed from Figure 4(b) that zinc-blende (ZB)/wurzite (WZ) polytypism and stacking faults may exist inside NPs, which is very common in patterned SA growth of III-V NWs/NPs compared with VLS growth. Further, no threading

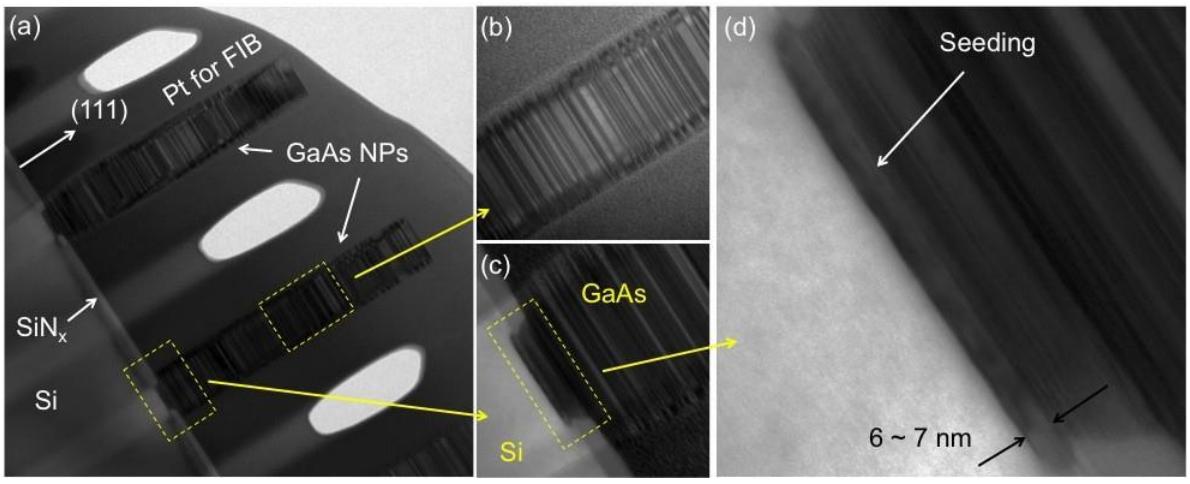


**Figure 3.** (a) Cross-sectional TEM image of the Zn-doped GaAs on Si with GaAs seeding layer grown at 600 °C for 5 s. (b) The zoom-in image of bulk GaAs NP section. (c) The zoom-in image of Si/GaAs interface and nanohole. (d) Further close-up detail of Si/GaAs interface.

dislocations and anti-phase domains (APDs) are found at Si/GaAs interface in Figure 3(d). It is also noted that the seeding layer was started grown beneath the $SiN_x$ mask and a wedged GaAs crystalline structure was formed. The thickness of such wedged layer is around 6 – 7 nm. It can be explained as following: during the sample preparation, $H_2O_2$ from Piranha and $O_2$ plasma oxidized the top Si surfaces inside the nanoholes, and the oxidized part was removed by BOE to formed the wedged opening. In order to accomplish high yield of vertical growth, another significant factor is to obtain a flat exposed Si top surface after sample preparation. If not, it is possible that the mix of (111)A and (111)B surface will be formed after TBA surface treatment right before seeding layer growth, which results in the inclined NP growth. For the future work, two improvements can be made to further increase the uniformity and NP material quality: (1) the NP growth temperature can be increased to reduce the density of stacking faults; and (2) a slight amount of antimony (Sb) can be added during NP growth to reduce ZB/WZ polytypism, which works for InAsSb NP growth on InAs substrates.

### D. Optical Characterization of GaAs Material Quality on Silicon

The optical properties of the GaAs NPs with different seeding layer temperature were compared. The samples grown at 450°C, 550°C, and 600°C were selected for the characterization due to their high uniformity and vertical yield. First, the PL characterization is shown in Figure 4, and the full-width-at-half-maximum (FWHM) of the PL peaks between 1.4 eV and 1.5 eV is plotted in the function of seeding layer temperature in the inset. The PL intensities are normalized in order to clearly compare the peak energies and FWHM. The diameter of laser spot on the samples is estimated at 7 $\mu m$, and around 200 NPs are covered. All PL spectra show two peaks – the one with higher energy is from band-to-band transition and the other with lower energy is from band-to-acceptor transition. The energies of band-to-band peaks for 450°C, 550°C and

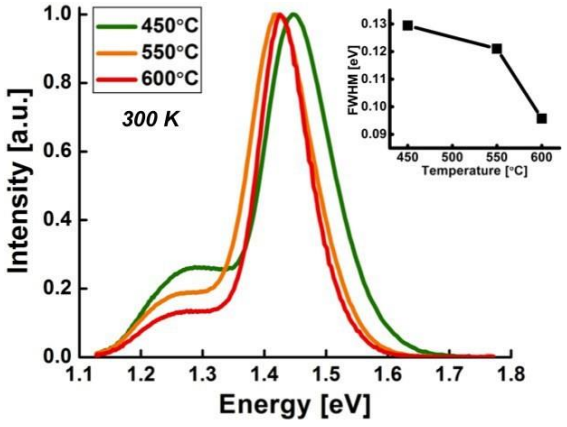


**Figure 4.** The PL spectra of p-GaAs on Si in the function of energy at 300 K. The three samples with different seeding layer growth temperature are compared. In the inset, the FWHM of peaks from GaAs band-to-band emission are given.

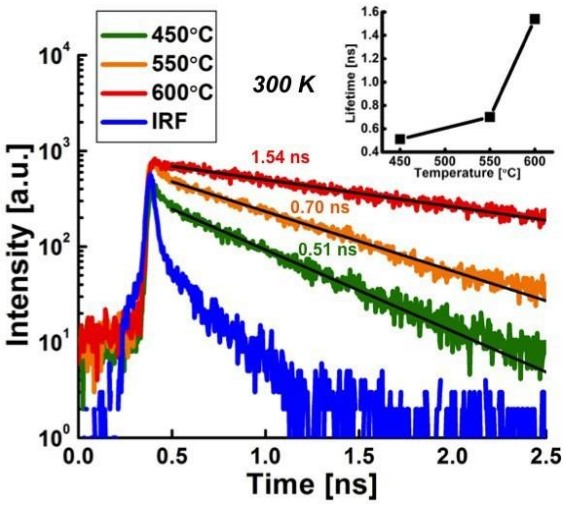


**Figure 5.** The TRPL spectra of p-GaAs on Si at 300 K. The three samples with different seeding layer

600°C seeding are 1.447 eV, 1.419 eV and 1.425 eV, respectively. The slight shift of the band gap energy from the theoretical value 1.424 eV may be due to the ZB/WZ polytypism. However, the NPs with 450°C seeding shows the largest shift with 20 meV from 1.424 eV compared with other two cases. Moreover, with the increase of seeding layer temperature from 450°C to 600°C, the FWHM is reduced from 129 meV to 98 meV.

The TRPL spectra of band-to-band recombination and the extracted lifetime are shown in Figure 5. The fast decay at the beginning in instrumental response function (IRF) is 30 ps, and the second part of decay is about 200 ps. Both decays are due to the Si SPADs, and the detector does not limit the total decay from NPs. To extract the lifetime, the NP signals from 0.5 ns to 2.5 ns were fitted by a single exponential decay $exp(-t/\tau)$. The fitting lifetimes of band-to-band recombination for 450°C, 550°C and 600°C seeding are 0.51 ns, 0.70 ns, and 1.54 ns, respectively. Therefore, the lifetime is largely affected by the seeding growth temperature. It is possible that the low-temperature nonstoichiometric GaAs seeding introduces more stacking faults and rotational twins into the NP segments. This may be also explained that more lattice vacancies are formed due to the Zn dopants with imperfect seeds. Compared with the reported lifetime of intrinsic GaAs NW/NP on Si, the Zn-doped GaAs with 600°C seeing layer gives comparable value. To the best of our knowledge, it is the first time that the long minority carrier lifetime of doped GaAs on Si is reported. In the future study, the electrical properties of doped GaAs NPs also need to be investigated.

**Conclusions and Outlook:**

The final year of this project has successfully developed and studied a growth technique that uses GaAs seeding layer as a transition between Si and III-V to achieve high-uniform NP growth on Si by SAE. The temperature during seeding layer growth is the factor to control the nucleantion to obtain over 99% yield of vertical growth. The threading dislocations and APDs are fully eliminated at Si/GaAs interface. Using PL and TRPL characterization, we compared that the optical properties of Zn-doped GaAs NPs grown with different seeding layer temperature. More studies need to be done to further improve GaAs material quality. We believe this seeding layer technique shows its potential to support the growth of GaAs-based ternary NPs on Si by using similar growth conditions on GaAs substrates. In conclusion, this work paves the way for the development of high-performance optoelectronics directly grown on Silicon substrates.

**Patents Derived from this Project:**

[1] A.C. Scofield, A. Lin, D.L. Huffaker, "Hybrid Si/III-V nanopillar optoelectronic devices", U.S. Provision Patent No. 62/019,234

**Publications Derived from this Project:**

[1] A. Scofield, A. Lin, M. Haddad, D.L. Huffaker, "Axial Diffusion Barriers in Near-Infrared Nanopillar LEDs," Nano Letters, 2014.

**References:**

[1] K. Sladek, V. Klinger, J. Wensorra, M. Akabori, H. Hardtdegen, and D. Grützmacher, "MOVPE of n-doped GaAs and modulation doped GaAs/AlGaAs nanowires," *J. Cryst. Growth*, vol. 312, no. 5, pp. 635–640, Feb. 2010.

[2] L. J. Lauhon, M. S. Gudiksen, and C. M. Lieber, "Semiconductor nanowire heterostructures.," *Philos. Trans. A. Math. Phys. Eng. Sci.*, vol. 362, no. 1819, pp. 1247–60, Jun. 2004.

[3] F. Léonard and a A. Talin, "Electrical contacts to one- and two-dimensional nanomaterials.," *Nat. Nanotechnol.*, vol. 6, no. 12, pp. 773–83, Dec. 2011.

[4] A. Scofield and A. Lin, "Composite axial/core-shell nanopillar light-emitting diodes at 1.3 um," *Appl. Phys. …*, vol. 053111, pp. 5–8, 2012.

[5] F. Glas, "Critical dimensions for the plastic relaxation of strained axial heterostructures in free-standing nanowires," *Phys. Rev. B*, vol. 74, no. 12, p. 121302, Sep. 2006.

[6] H. Ye, P. Lu, Z. Yu, Y. Song, D. Wang, and S. Wang, "Critical thickness and radius for axial heterostructure nanowires using finite-element method," *Nano Lett.*, vol. 9, no. 5, pp. 1921–5, May 2009.

[7] P. D. Dapkus and J. J. Jewell, "1.2-μm GaAsP/InGaAs strain compensated single-quantum-well diode laser on GaAs using metal-organic chemical vapor deposition," *IEEE Photonics Technol. Lett.*, vol. 11, no. 12, pp. 1572–1574, Dec. 1999.

[8] T. Maruyama, D. -a. Luh, a. Brachmann, J. E. Clendenin, E. L. Garwin, S. Harvey, J. Jiang, R. E. Kirby, C. Y. Prescott, R. Prepost, and a. M. Moy, "Systematic study of polarized electron emission from strained GaAs⁄GaAsP superlattice photocathodes," *Appl. Phys. Lett.*, vol. 85, no. 13, p. 2640, 2004.

[9] D. C. Bertolet, J. Hsu, F. Agahi, and K. E. I. M. A. Y. Lau, "Critical Thickness of GaAs / InGaAs and AIGaAs / GaAsP Strained Quantum Wells Grown by Organometallic Chemical Vapor Deposition," vol. 19, no. 9, 1990.

[10] P. Senanayake, A. Lin, G. Mariani, J. Shapiro, C. Tu, A. C. Scofield, P.-S. Wong, B. Liang, and D. L. Huffaker, "Photoconductive gain in patterned nanopillar photodetector arrays," *Appl. Phys. Lett.*, vol. 97, no. 20, p. 203108, 2010.

1.

**1. Report Type**

Final Report

**Primary Contact E-mail**

**Contact email if there is a problem with the report.**

huffaker@ee.ucla.edu

**Primary Contact Phone Number**

**Contact phone number if there is a problem with the report**

310-302-7841

**Organization / Institution name**

University of California Los Angeles

**Grant/Contract Title**

**The full title of the funded effort.**

Nanopillar Photonic Crystal Lasers for Tb/s Transceivers on Si

**Grant/Contract Number**

**AFOSR assigned control number. It must begin with "FA9550" or "F49620" or "FA2386".**

FA9550-12-1-0052

**Principal Investigator Name**

**The full name of the principal investigator on the grant or contract.**

Diana Huffaker

**Program Manager**

**The AFOSR Program Manager currently assigned to the award**

Gernot Pomrenke

**Reporting Period Start Date**

04/01/2014

**Reporting Period End Date**

03/31/2015

**Abstract**

The objective of this project is the development of materials and devices to be used in next-generation Tb/s optical transceivers on Silicon substrates. This project has focused on a unique approach to growth of III-V emitters via selective-area epitaxy (SAE). The use of SAE growth at nanoscale dimensions avoid defect formation due to lattice mismatch by allowing strain relief in the lateral direction. Following the development of waveguide-coupled NP optoelectronic devices which was the focus of the second year of the project, the final year focused on the integration of the NP devices on Silicon substrates. The GaAs seeding layer was studied to achieve high vertical yield and high-uniformity GaAs nanopillars on Si(111) substrates by SAE. Seeding layer growth temperature was optimized to obtain over 99% yield of vertical growth. The nanopillars were passivated by in-situ AlGaAs shells to reduce the surface recombination. No threading dislocation and anti-phase domains were observed at Si/GaAs interface by transmission electron microscopy. Moreover, the optical properties of NPs were measured by photoluminescence and time-resolved photoluminescence at room temperature to investigate the effects of seeding layer parameters. Under the optimum conditions, it was found that GaAs NPs on Silicon can have carrier recombination lifetimes in excess of 1 ns, which is comparable to NPs grown on GaAs substrates.

**Distribution Statement**

**This is block 12 on the SF298 form.**

Distribution A - Approved for Public Release

**Explanation for Distribution Statement**

**If this is not approved for public release, please provide a short explanation. E.g., contains proprietary information.**

**SF298 Form**

**Please attach your SF298 form. A blank SF298 can be found here. Please do not password protect or secure the PDF The maximum file size for an SF298 is 50MB.**

SF298_Huffaker_Y3.pdf

**Upload the Report Document. File must be a PDF. Please do not password protect or secure the PDF . The maximum file size for the Report Document is 50MB.**

AFOSR_Y3_Report_Huffaker.pdf

**Upload a Report Document, if any. The maximum file size for the Report Document is 50MB.**

**Archival Publications (published) during reporting period:**

A. Scofield, A. Lin, M. Haddad, D.L. Huffaker, “Axial Diffusion Barriers in Near-Infrared Nanopillar LEDs,” Nano Letters, 2014

**Changes in research objectives (if any):**

**Change in AFOSR Program Manager, if any:**

**Extensions granted or milestones slipped, if any:**

**AFOSR LRIR Number**

**LRIR Title**

**Reporting Period**

**Laboratory Task Manager**

**Program Officer**

**Research Objectives**

**Technical Summary**

**Funding Summary by Cost Category (by FY, $K)**

| | Starting FY | FY+1 | FY+2 |
|---|---|---|---|
| Salary | | | |
| Equipment/Facilities | | | |
| Supplies | | | |
| Total | | | |

**Report Document**

**Report Document - Text Analysis**

**Report Document - Text Analysis**

**Appendix Documents**

## 2. Thank You

**E-mail user**

Jun 30, 2015 17:48:07 Success: Email Sent to: huffaker@ee.ucla.edu